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ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/994,574	WHEELER ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,10-13,15,18,21-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,10-13,15,18,21-23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to an Amendment filed November 17, 2006. Claims 3, 9 and 20 were cancelled. No claims were added. Claims 1, 4 - 7, 10 - 13, 15, 18, 21 - 23 and 25 - 27 are pending. Claims 1, 4 - 7, 10 - 13, 15, 18, 21 - 23 and 25 - 27 have been examined. Claims 1, 4 - 7, 10 - 13, 15, 18, 21 - 23 and 25 - 27 have been rejected.

2. **The Examiner would like to thank the Applicant for the well-presented response, which was useful in the examination process.** The Examiner appreciates the effort to perform a thorough analysis and make appropriate arguments and amendments.

3. This Office Action is NON-final due to new rejections under 35 USC § 101 as a result of training.

Response to Arguments

4. Regarding **claim 7** objected to for minor informalities:

4.1. The Examiner thanks the Applicant for the amendment, and especially for the reference to the MPEP, which will be useful in future examinations. However, even though the order to the limitations may not be important, the claim would have still needed to be amended to avoid an antecedent issue, which is corrected by the amendment.

5. Regarding **claim 1** rejected under 35 U.S.C. § 103:

5.1. Applicants' arguments have been fully considered, but are not persuasive, as follows. Accordingly, the rejections are maintained.

5.2. The Applicant argues:

5.3. The rejection contends that it would have been obvious for one of ordinary skill to combine Yumoto, Yamagishi, and the IEEE Std. 1364-1995 to arrive at a logic design module that is operable to update the logic design and to indicate design discrepancies in the logic design, as recited in claim 1. Applicant respectfully disagrees.

5.4. In this regard, Yumoto describes a parameterized method for designing data driven media processors (DDMP). See, e.g., *Yumoto,* Title. FIGS. 5-12 of Yumoto illustrate the various hierarchical-levels of a DDMP. *See, e.g., Yumoto*, paras. [0038]-[0045]. Elements at these various hierarchical levels of a DDMP can be changed by a user selection of a <u>predefined set of values for a collection of parameters.</u> *See, e.g., Yumoto*, para. [0090]-[0092] (describing that three different "value units," each of which includes a variety of associated values, can be selected by a user); para. [0085] (describing that the data width bit and number of parallel data

stored in a memory unit are "preset"). *See also Yumoto, FIG.* 13 (showing predefined parameter values for the "min condition," the "typ condition," and the "max condition"); para. [0087] (describing that the elements required to design other functional blocks are "extracted in advance" and parameterized); para. [0089] (describing that Yumoto's parameterize RTL design tool automatically produces an RTL descriptor file based on such "predetermined parameters").

5.5. Such predetermined sets of values can be selected for "each functional block" of a DDMP. *See, e.g., Yumoto*, para. [0101]-[0103]. Examples of prototype library files of such functional blocks are shown in Yumoto's FIGS. 15-17. *See, e.g., Yumoto*, para. [0048]-[0050]; [0093]. Such prototype library files are used with a predetermined sets of values to produce RTL descriptions as shown in FIGS. 18-20. *See, e.g., Yumoto*, para. (0093]; [00511-f00531; (00941. As best understood by applicant, the inputs or outputs of the functional blocks are not changed through the user selection of different predetermined sets of values. *See, e.g., Yumoto*, FIGS. 18-20.

5.6. Against this backdrop, the rejection contends that it would have been obvious to add **IEEE Std.** 1364-1995's comparison between bit lengths of port expressions in instance arrays and bit lengths in single instance ports so that Yumoto's parameterized method could indicate design discrepancies in a logic design. Applicant respectfully disagrees.

5.7. To begin with, Applicant is at a loss to understand how the comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports in IEEE Std. *1364-1995* indicate design discrepancies. To the best of applicants' understanding, the IEEE Std. 1364-1995 comparison *determines* how single instance ports/terminals in an instantiated module are to be connected to ports/terminals in an instance-array port expression. *See* ***IEEE Std. 1364-1995,*** **page** *59*, line *5-9*. In other words, the IEEE Std. 1364-1995 comparison appears to be part of the *generation* of a logic design, rather than an indication of design discrepancies in a logic design, as recited in claim 1.

5.7.1. The Examiner respectfully replies:

5.7.2. The intention of the recited portion of IEEE Std. 1364-1995 (page 59, lines 1 - 25) is to satisfy the limitation, "to indicate design discrepancies in the logic design resulting from modifications to the values of the signal parameters". The recited portion recites that too many or too few bits to connect all the instances shall be considered an error, which appears to suggest the limitation, since an ordinary artisan would expect the Verilog compiler to issue an error message indicating the design discrepancy between signal parameters. Further, the Examiner maintains that an ordinary artisan would have known that a Verilog compiler would indicate design discrepancies in a logic design resulting from mismatched signal parameters, such as connecting an 8 bit signal to a 4 bit signal. When the design of Yumoto was compiled by a Verilog compiler (a logic design module operable to generate a logic design), the Verilog compiler would have indicated design discrepancies in the logic design resulting from

mismatched signal parameters, and thus, the ordinary artisan would have naturally combined the art.

5.8. The Applicant argues:

5.9. Moreover, as discussed above, Yumoto's users select a predefined set of values for a collection of parameters for "each functional block" of a DDMP. It would seem unlikely that such predefined set of values could potentially have internal design discrepancies of the type that would require checking. Rather, it would appear likely that the predefined sets of values for each functional block would be defined to be internally consistent, i.e., without design discrepancies. No design discrepancies in the logic design would be likely to result from the user selection of such an internally consistent set of values. Accordingly, applicant submits that it would not be obvious for one of ordinary skill to add the IEEE Std. 1364-1995 comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports to check consistency of Yumoto's functional blocks.

5.9.1. The Examiner respectfully replies:

5.9.2. The Examiner respectfully disagrees. Perhaps in a completely debugged design, the predefined sets of values for each functional block would be defined to be internally consistent, but any change to the logic design could potentially introduce errors that would want to be identified through identifying discrepancies. Further, certain combinations of selected predefined values could be incompatible by causing discrepancies, and these combinations would want to be discovered by finding design discrepancies. Therefore, it would seem obvious to combine the art of Yumoto with the art of IEEE 1364-1995.

5.9.3. Further, Yumoto appears to indicate that individual values can be modified. For example, refer to page 6, paragraph [0102], which appears to indicate that individual values can be modified.

6. Regarding **claims 7 and 18** rejected under 35 U.S.C. § 103:

6.1. Applicants' arguments have been fully considered, but are not persuasive, as follows. Accordingly, the rejections are maintained.

6.2. Applicant's arguments for claims 7 and 18 are analogous to the arguments for claim 1. The Examiner's replies to claim 1 apply to claims 7 and 18.

7. Regarding **claim 15** rejected under 35 U.S.C. § 103:

7.1. Applicants' arguments have been fully considered, but are not persuasive, as follows. Accordingly, the rejections are maintained.

7.2. The Applicant argues:

7.3. As amended, claim 15 relates to an apparatus that includes a central database accessible by one or more users, modification logic to allow a user to modify the values associated with the identifiers individually, and an interface to convey the identifiers and the associated values from the central database to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit. The central database includes a collection of identifiers of one or more bit width signal parameters and values associated with each of the identifiers of the bit width signal parameters.

7.4. As discussed above, Yumoto's parameterized method uses predefined sets of values for a collection of parameters to change elements for each functional block of a DDMP. Yumoto does not allow a user to modify values associated with the identifiers individually. Rather, multiple values are always modified as a set.

7.5. Yamagishi does nothing to remedy this deficiency in Yumoto. Indeed, Yamagishi has nothing to do with modification logic to allow a user to modify the values associated with identifiers.

7.6. Accordingly, applicant submits that claim 15 is not obvious over the combination of Yumoto and Yamagishi. Applicant therefore requests that the rejection of claim 15 be withdrawn.

7.6.1. The Examiner respectfully replies:

7.6.2. The Examiner respectfully disagrees with the Applicant's assertion that Yumoto does not allow a user to modify values associated with the identifiers individually. For example, refer to page 6, paragraph [0102], which appears to indicate that individual values can be modified. Accordingly, the premise of the Applicant's argument appears to be overcome, and therefore, the conclusion does not follow.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1, 4 - 7, 10 - 13, 15, 18, 21 - 23 and 25 - 27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

9.1. Regarding claims 1, 4 - 6 and 26 - 27, the recited system appears to contain software, such as a logic design module, which appears to be an abstract idea. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claims do not appear to produce a tangible result needed to support a practical application. Further, several factors appear to prevent a tangible result. First, there does not appear to be a processor integrated with the software that would allow the functionality of the software to be realized. Second, the logic design module is operable to perform actions, but does not appear to actually perform the actions.

9.2. Regarding claims 7 and 10 - 13, the recited method appears to perform abstract operations, such as modifying computer code. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claims do not appear to produce a tangible result needed to support a practical application. The actions of updating computer code and indicating design discrepancies do not appear to produce a tangible result.

9.3. Regarding claim 15, the recited apparatus appears to perform abstract operations, such as changing a bit width. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claim does not appear to produce a tangible result needed to support a practical application. Further, the apparatus appears to contain software (i.e., a logic design module), but there does not appear to be a processor integrated with the software that would allow the functionality of the software to be realized, which prevents a tangible result.

9.4. Regarding claims 18, 21 - 23 and 25, the recited machine-accessible medium appears to contain abstract operations, such as updating a logic design. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claims do not appear to produce a tangible result needed to support a practical application. The actions of updating a logic design and indicating design discrepancies do not appear to produce a tangible result.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. **Claims 1, 4 - 6, 7, 10 - 13, 18, 20 - 23** and **25 - 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference), further in view of IEEE Verilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

12.1. The art of Yumoto is directed to logic design systems *(page 1, paragraph [0002])*.

12.2. The art of Yamagishi is directed to logic design systems *(page 13.2.1, Abstract, and section 1 Introduction)*.

12.3. The art of IEEEVerilog is directed to logic design *(page iii, section Introduction)*.

12.4. Regarding **claim 1**:

12.5. Yumoto appears to teach:

12.5.1. a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit, wherein the logic design includes labels *(figure 15, it would have been obvious that a logic design module was used to build the displayed code, wherein the logic design module was a tool such as SILOS III from Simucad; and page 2, paragraph [0029])*.

12.5.2. a collection of modifiable values of signal parameters that are accessible by the logic design module, wherein the values of signal parameters are associated with the labels in the logic design *(figure 14; and figure 15,it would have been obvious that the included file np1_param_define.v contained bit width signal parameters with labels cst1_packet_in_width and cst1_packet_out_width, and it would have been obvious that the signal parameters were accessible by the logic design module; and page 2, paragraph [0029])*.

12.5.3. The logic design module is operable to update the logic design to reflect modification of the values of the signal parameters by modifying the logic design to be compatible with the modified values of the signal parameters *(figure 15, it would have been obvious that compiling the Verilog code would have used the signal parameters in file np1_param_define.v to modify the signal widths to be compatible with the modified values of the signal parameters; and page 2, paragraph [0029])*.

12.6. Yumoto does not specifically teach:

12.6.1. *a central database integrated with the logic design module*.

12.6.2. The logic design module is operable to update the logic design to reflect modification of the signal parameters ***in the central database***.

12.6.3. to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically.

12.7. Yamagishi appears to teach:

12.7.1. a central database integrated with the logic design module *(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)*.

12.8. IEEEVerilog appears to teach:

12.8.1. to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically (*page 59, lines 1 - 25*).

12.8.1.1. Regarding (*page 59, lines 1 - 25*); it would have been obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

12.9. Yumoto and Yamagishi are analogous art because they are both directed to the art of logic design systems.

12.10. Yumoto and IEEEVerilog are analogous art because they both contain the art of logic design.

12.11. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*; and the

expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

12.12. The motivation to use the art of IEEEVerilog with the art of Yumoto would have been the knowledge of the ordinary artisan that indicating design discrepancies would save time and effort by allowing the ordinary artisan to correct the discrepancies and thereby make the logic design functional.

12.13. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEEVerilog with the art of Yumoto to produce the claimed invention.

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12.14. Regarding **claim 4**:

12.15. Yumoto appears to teach indicating a bit width *(figure 15, input signal d has a bit width)*.

12.16. Yumoto does not specifically teach indicating a bit width *error*.

12.17. IEEEVerilog appears to teach indicating a bit width error *(page 59, lines 1 - 25)*.

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12.18. Regarding **claim 5**:

12.19. Yumoto appears to teach:

12.19.1. the signal parameters characterize a signal bit width (*figure 15, input signal d, element cst1_packet_in_width*).

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12.20. Regarding **claim 6**:

12.21. Yumoto appears to teach:

12.21.1. the signal parameters characterize a signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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12.22. Regarding **claim 26**:

12.23. Yumoto appears to teach:

12.23.1. the signal parameters define characteristics that characterize multiple bits of a multiple bit signal (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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12.24. Regarding **claim 27**:

12.25. Yumoto appears to teach:

12.25.1. the signal parameter defines a characteristics that characterizes multiple bits of a multiple bit signal (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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12.26. Regarding **claim 7**:

12.27. Yumoto appears to teach:

12.27.1. receiving an assignment of a value to a signal parameter *(figure 15; it would have been obvious that element cst1_packet_in_width received an assigned value)*

12.27.2. Maintaining the value of the signal parameter in association with an identifier of the signal parameter *(figure 14; it would have been obvious that the value of a signal parameter was maintained)*.

12.27.3. Using the identifier of the signal parameter to identify a first position in computer code for a logic design forming part of an electrical circuit *(figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would use the identifier of the signal parameter to identify all positions in the computer code where th eidentifier was used)*.

12.27.4. Modifying the computer code at the first position to reflect the value (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

12.27.5. Using the identifier of the signal parameter to identify a second position in computer code for the logic design *(figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would use the identifier of the signal parameter to identify all positions in the computer code where the identifier was used)*.

12.27.6. Receiving an updated value of the signal parameter (*Abstract; and figure 14; and figure 15, element cst1_packet_in_width; and page 2, paragraph [0029]; it would have been obvious that an updated value of the signal parameter was received*).

12.27.7. Modifying the computer code at the second position to reflect the value (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

12.27.8. Updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would update all positions in the computer code for the logic design to reflect the updated value of the signal parameter*).

12.28. Yumoto does not specifically teach:

12.28.1. Maintaining the defined signal value *in a central database*.

12.28.2. Using the identifier of the signal parameter maintained *in the central database* .

12.28.3. Receiving an updated value of the signal parameter *in the central database*.

12.28.4. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

12.29. Yamagishi appears to teach:

12.29.1. a central database integrated with a logic design module (*pages 13.2.2 and 13.2.3, section 2.2 Database FALNET*).

12.30. IEEEVerilog appears to teach:

12.30.1. indicating design discrepanciesoccurring in the logic design that result from updating the value of the defined signal parameter automatically (*page 59, lines 1 - 25*).

12.30.1.1. Regarding (*page 59, lines 1 - 25*); it would have been obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

12.31. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEEVerilog with the art of Yumoto to produce the claimed invention.

12.32. Regarding **claim 11**:

12.32.1. Yumoto appears to teach:

12.32.1.1. the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

12.33. Regarding **claim 12**:

12.33.1. Yumoto appears to teach:

12.33.2. the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

12.34. Regarding **claim 13**:

12.34.1. Yumoto appears to teach:

12.34.2. the signal parameter characterizes a bit field and the value includes a value for the bit field (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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12.35. Regarding **claim 10**:

12.35.1. Yumoto does not specifically teach:

12.35.1.1. graphically indicating a bit width error.

12.35.2. Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

12.35.3. Yamagishi appears to teach graphically indicating errors (**figure 1**).

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12.36. Regarding **claim 18**:

12.37. Yumoto appears to teach:

12.37.1. Receiving a value of a signal parameter that characterizes multiple bits of a multiple bit signal *(figure 14, element GEN_WIDTH; it would have been obvious that a value was received in order to enter the value)*.

12.37.2. Maintaining the value of the signal parameter *(figure 14, element GEN_WIDTH)*.

12.37.3. Using the value of the signal parameter that is maintained, in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal *(figure 15, element cst1_packet_in_width)*.

12.37.4. Receiving an update to the value of the signal parameter (page 2, paragraph [0029]).

12.37.5. updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated signal parameter (*figure 15; it would have been obvious that compiling the Verilog code would have updated the logic design by modifying the logic design to be compatible with the updated signal parameter, since the parameter cst1_packet_in_width would be updated with a value from the include file np1_param_define.v*).

12.38. Yumoto does not teach specifically teach:

12.38.1. Using the defined signal parameter *that is maintained in the central database* in computer code for a logic design forming part of an electrical circuit.

12.38.2. Maintaining the value of signal parameter *in a central database*.

12.38.3. Using the value of the signal parameter that is maintained *in the central database*.

12.38.4. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

12.39. Yamagishi appears to teach:

12.39.1. Maintaining logic design data *in a central database* (*page 13.2.1, section 2 FALcyber, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET*).

12.40. IEEEVerilog appears to teach:

12.40.1. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically (*page 59, lines 1 - 25*).

12.41. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than

other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

12.42. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEVerilog with the art of Yumoto to produce the claimed invention.

12.43. Regarding **claim 22**:

12.43.1. Yumoto appears to teach:

12.43.1.1. the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

12.44. Regarding **claim 23**:

12.44.1. Yumoto appears to teach:

12.44.1.1. the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

12.45. Regarding **claim 25**:

12.45.1. Yamagishi appears to teach:

12.45.1.1. permitting one or more users to access the central database *(page 13.2.1, figure 1)*.

12.46. Regarding **claim 20**:

12.47. Yumoto does not specifically teach automatically indicating design discrepancies in the logic design that result from updating the value of the defined signal parameter.

12.48. IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the signal parameters *(page 59, lines 1 - 25)*.

12.48.1. Regarding *(page 59, lines 1 - 25)*; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

12.49. Yumoto and IEEEVerilog are analogous art because they both are directed to the problem of logic design.

12.50. Regarding **claim 21**:

12.50.1. Yumoto does not specifically teach:

12.50.1.1. graphically indicating a bit width error.

12.50.2. Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

12.51. Yamagishi appears to teach graphically indicating errors (**figure 1**).

==

13. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

13.1. Regarding **claim 15**:

13.2. Yumoto appears to teach:

13.2.1. a collection of identifiers of one or more bit width signal parameters *(figure 14)*.

13.2.2. values associated with each of the identifiers of the bit width signal parameters *(figure 14)*.

13.2.3. modification logic to allow a user to modify the values associated with the identifiers individually (*page 6, paragraph [0102]; and figure 14; it would have been obvious that a tool such as a text editor would allow the user to modify the values associated with the identifiers*).

13.2.4. an interface to convey the identifiers and the associated values to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit (*figure 15, element cst1_packet_in_width; it would have been obvious that there was an interface, such as a Verilog compiler, between the include file npl_param_define.v and the code in order to identify where the logic design was to be changed*);

13.3. Yumoto does not specifically teach:

13.3.1. *A central database accessible by one or more users.*

13.3.2. One or more signal parameters defined *in the central database*.

13.3.3. an interface to convey the identifiers and the associated values from *__the central database__*.

13.4. Yamagishi appears to teach a central database accessible by one or more users *__(page 13.2.1, figure 1, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)__*.

13.5. Yumoto and Yamagishi are analogous art because they are both directed to the art of logic design systems.

13.6. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *__(page 13.2.3, left-side of page, lines 1 - 3)__*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *__(page 2, second paragraph)__*.

13.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Yumoto to produce the claimed invention.

14. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Conclusion

15. The following prior art is relevant to the Applicant's disclosure:
    - **15.1.** Cismas (U.S. Patent 6,996,799) teaches parameterized signals.
    - **15.2.** Sharma (U.S. Patent 5,841,663) teaches parameterized HSL modules.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.
17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

12/29/06

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER